



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

Address: COMMISSIONER FOR PATENTS

P.O. Box 1450

Alexandria, Virginia 22313-1450

www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/743,230	12/21/2003	Nikholas Hubbard	200208-474-1	7631
22879 7590 07/09/2009 HEWLETT PACKARD COMPANY P O BOX 272400, 3404 E. HARMONY ROAD INTELLECTUAL PROPERTY ADMINISTRATION FORT COLLINS, CO 80527-2400				
EXAMINER DEBERADINIS, ROBERT L				
ART UNIT 2836		PAPER NUMBER		
NOTIFICATION DATE 07/09/2009		DELIVERY MODE ELECTRONIC		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

JERRY.SHORMA@HP.COM

ipa.mail@hp.com

jessica.l.fusek@hp.com

### Office Action Summary

**Application No.**

10/743,230

**Applicant(s)**

HUBBARD ET AL.

**Examiner**

Robert DeBeradinis

**Art Unit**

2836

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 19 April 2009.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-34 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-34 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-850)
- Paper No(s)/Mail Date 12/21/03
- 4) ☐ Interview Summary (PTO-413)
- Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Inventor's Patent Application
- 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

***Response to Arguments***

The Applicant's argument is persuasive. The restriction requirement is withdrawn.  
All claims considered.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1,3-11,13-24,26-30,32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over MIYAZAKI et al. 5,297,015 in view of TUSTISON et al. 20040258141.

CLAIMS 1,24,26,29,30,32-34

MIYAZAKI et al. discloses a power supply control system including a variable power converter for converting electric power from a power supply to a load into that of a specification required by the load in response to a power specification information source provided on the load side (abstract), wherein the system includes an interconnect to carry direct current; an electronic device connectable to the interconnect to receive DC and having the means for the power supply to sense the power specification information provided on the load side.

MIYAZAKI et al. does not disclose interconnect to receive DC and having a communication circuit to transmit signals over interconnect; and a power supply connectable to interconnect to provide the DC to the electronic device and having a decoder circuit to decode the signals received over the interconnect from the electronic device.

TUSTISON et al. discloses a power line modem interface includes a modem that modulates an RF signal with digital data and demodulates an RF signal to recover digital data. A filter is connected to the modem and to a DC power line that supplies power to a local power supply. The filter couples the RF signals from the modem to the DC power line and filters the RF signals out of the local power supply (abstract).

It would have been obvious to one having ordinary skill in the art at the time of the invention to have modified the power supply control system with the modem interface so that signals received over the interconnect from the electronic device are decoded in the power supply to control the power supplied to the load in response to power specification information source provided on the load side.

CLAIMS 3,4,5,22,28

MIYAZAKI et al. in view of TUSTISON et al. disclose the system of claim 1.

MIYAZAKI et al. discloses high frequency PCM and PSK modulation but is silent as to PWM which is another well known modulation method.

It would have been an obvious matter of design choice to select the preferred signal to communicate to the controlled device to control the power supply, since

applicant has not disclosed that the communication signal choice solves any stated problem.

CLAIMS 6,8,13,21,27

MIYAZAKI et al. in view of TUSTISON et al. disclose the system of claim 1.

TUSTISON discloses filter to isolate the communication signals from the device power.

CLAIMS 7,14,23

MIYAZAKI et al. in view of TUSTISON et al. disclose the system of claim 1 except wherein the electronic device is an image-forming device. This is an intended use for the supply, it has been held that recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus satisfying the claimed structure limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987).

CLAIMS 9,10

MIYAZAKI et al. in view of TUSTISON et al. discloses the claimed invention except for the power supply and interconnect are external to the electronic device.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have arrange the parts any way desired, since it has been held that rearranging parts of an invention involves only routine skill in the art. In re Japikse, 86 USPQ 70.

CLAIMS 11,15,16-19

MIYAZAKI et al. in view of TUSTISON et al. discloses a system comprising a direct current interconnect (see above); an electronic device having a principal functionality and connectable to the interconnect to receive DC and comprising: one or more components to provide functionality of the electronic device ; a pulse-width modulation (PWM) communication circuit to transmit high frequency PWM signals over the interconnect (see claim 3 rejection above); an inductive isolating component to substantially isolate the high frequency PWM signals from the one or more components of the electronic device (passive filter); and a power supply connectable to the interconnect to convert alternating current (AC) from a power source to DC for the electronic device and comprising: one or more components to convert the AC to the DC according to one or more parameters; a decoder circuit (line modem interface) to decode the high frequency PWM received over the interconnect from the electronic device into one or more parameters; an inductive isolating component to substantially isolate the high frequency PWM signals from the one or more components of the power supply (refer to passive filter above).

#### CLAIM 20

MIYAZAKI et al. in view of TUSTISON et al. discloses the electronic device of claim 16, TUSTISON et al. discloses power line modem interface modulates RF signal with digital data (abstract). It is obvious that communication circuit comprises a signal generator to generate the RF and digital signals.

Claims 2,12,25,31 are rejected under 35 U.S.C. 103(a) as being unpatentable over MIYAZAKI et al. 5,297,015 in view of TUSTISON et al. 20040258141 in further view of POTEGA 6,459,175.

CLAIMS 2,12,25,31

MIYAZAKI et al. in view of TUSTISON et al. disclose the system of claim 1.

The above references do not disclose wherein the power supply further has a communication circuit to transmit additional communication signals over the interconnect, and the electronic device further has a decoder circuit to decode the additional communication signals received over the interconnect from the power supply.

POTEGA discloses a master control unit receives inputs from each of a plurality of power supplies and controls the delivery and supply of power being supplied to the power supplies.

It would have been obvious to one having ordinary skill in the art at the time of the invention to have modified the power supply to have the additional communication signals to for a power supply grid (abstract).

Any inquiry concerning this communication should be directed to Robert L. DeBeradinis whose number is (571) 272-2049. The Examiner can normally be reached Monday-Friday from 8:30 am to 5:00 pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Rexford Barnie, can be reached on (571) 272-7492. The Fax phone number for this Group is (571) 272-8300.

Application/Control Number: 10/743,230

Page 7

Art Unit: 2836

RLD

JUNE 25, 2009

/Robert DeBeradinis/

Primary Examiner, Art Unit 2836